REMARKS

Claims 1-28 are pending in this application.

In the Office Action, claims 1, 3, 4, 15-17, 19, 26 and 28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,228,036 (Okamoto et al.) in view of U.S. Patent Publication No. 2003/0161349 (Marutani). Claims 6-14 have been allowed. Claims 2, 5, 18, 20-25 and 27 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

Applicant thanks the Examiner for allowing claims 6-14 and indicating that claims 2, 5, 18, 20-25 and 27 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35 U.S.C. § 103 Rejections

Claims 1, 3, 4, 15-17, 19, 26 and 28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Okamoto et al. in view of Marutani. Applicant respectfully traverses these rejections.

Okamoto et al. discloses a frame synchronization stabilizer for stabilizing frame synchronization of received data that has a generation circuit for generating a reference pattern which is the same as a predetermined frame synchronization pattern contained in data being

transmitted. The stabilizer further has a comparison circuit for comparing, bit by bit, a data pattern in a synchronization pattern area of each frame of the received data with the reference pattern from a generation circuit. The comparison circuit outputs a mismatch pulse each time when a mismatch bit is detected by the comparison, and outputs a match pulse each time when it is detected that the pattern is fully matched with the reference pattern. The number of the mismatch pulses from the comparison circuit is counted by a first counter. The first counter outputs an out-of frame detection signal when a counted value exceeds a particular value and is reset based upon the match pulse from the comparison circuit.

Marutani discloses a synchronization protecting and setting system for signals received in a radio base station whereby a protection of synchronized word SW detected in a first synchronized word detecting window AP1 can be maintained in a second synchronized word detecting window AP2.. The synchronization protecting and setting method for signals received in a radio base station includes a first means generating a first synchronized word detecting window, which covers a position of synchronized word in a reception signal for a reference timing for transmission in the radio base station; a second means generating a second synchronization word detecting window, which covers the position of the synchronized word in the first synchronized word detecting window, a synchronized word detecting means detecting the synchronized word in the first or second synchronized word detecting window; and a control

means resetting a position of the second synchronized word detecting window in the first synchronized word detecting window, in a predetermined condition.

Regarding claims 1 and 15, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose suggest or render obvious the limitations in the combination of each of these claims of, *inter alia*, comparing a synchronization detection threshold value set for each section of a time period in which a quality of a pilot is measured and a pilot bit error rate calculated for each section, or judging a synchronization detection based on a result of the comparing. The Examiner asserts that Okamoto et al. discloses comparing a synchronization detection threshold value set for each section of a time period in which a quality of signal is measured, at col. 2, lines 61-65. However, these portions merely disclose that to present an out of frame due to a disturbance over the transmission line, the probability Perr should satisfy the condition that Perr ‹ X, where X is a threshold value of synchronization determination. This is not comparing a synchronization detection threshold value set for each section of a time period in which a quality of a pilot is measured, as recited in the claims of the present application. These portions merely disclose that the probability of occurrence of an out of frame due to a bit error (Perr) should be less than a threshold value of synchronization. These portions do not disclose or suggest comparing a synchronization detection value set for each section of a time period.

Further, the Examiner asserts that Okamoto et al. discloses a bit error rate calculated for each section, at col. 3, lines 10-13. However, these portions merely disclose an example where the size of the mismatched counter is adjusted due to the fact that the reception side cannot freely set the bit length K and the bit error rate P of the synchronization pattern. These portions have nothing to do with a bit error rate calculated for each section, as recited in the claims of the present application. Further, these portions do not disclose or suggest anything related to a pilot error rate.

The Examiner admits that Okamoto et al. fails to disclose or suggest an uplink synchronization detection and a measured signal being a pilot signal, but asserts that Marutani discloses these limitations in paragraphs 28 and 33. However, these portions merely disclose that the radio base station includes a synchronization section having an AP1 generator which generates a first synchronized word detecting window AP1(c) and that the synchronized word is necessary to establish a timing of receiving signals in the base station, and the color code CC is an interference counter-measure code allocated in each cluster, which is a frequency repeating unit, for distinguishing radio signals transmitted from an interference station. This is not an uplink synchronization detecting that includes comparing a synchronization detection threshold value set for each section of a time period in which a quality of a pilot is measured, and a pilot bit error rate calculated for each section, as recited in the claims of the present application.

These portions do not disclose or suggest performing a comparison, quality of a pilot, or a pilot error rate being calculated.

Further, Applicant submits that one of ordinary skill in the art would have no motivation to combine Okamoto et al., which relates to frame synchronization where a comparison circuit performs a comparison bit by bit, with Marutani that relates to synchronization for signals received in a radio base station that includes a synchronized word detecting means detecting the synchronized word in the first or second synchronized word detecting window. The methods of these two references conflict. Further, this combination fails to achieve the limitations in the claims of the present application.

Regarding claims 3, 4, 16, 17, 19, 26 and 28, Applicant submits that these claims are dependent on one of independent claims 1 and 15 and, therefore, are patentable at least for the same reasons noted previously regarding these independent claims.

Accordingly, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose suggest or render obvious the limitations in the combination of each of claims 1, 3, 4, 15-17, 19, 26 and 28 of the present application. Applicant respectfully requests that these rejections be withdrawn and that these claims be allowed.

CONCLUSION

In view of the foregoing remarks, Applicant submits that claims 1-28 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, Frederick D. Bailey, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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